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Reg. No. : .....

ode No. : 30314 E Sub. Code : SMPH 61

. (CBCS) DEGREE EXAMINATION, APRIL 2022

Sixth Semester

Physics — Core

DIGITAL ELECTRONICS

(For those who joined in July 2017 onwards)

Three hours Maximum : 75 marks

PART A — (10 × 1 = 10 marks)

Answer ALL questions.

The hexadecimal number corresponding to the binary number $(11110010)_2$ is

a) F5 (b) C2

c) F2 (d) C5

The gray code corresponding to binary $(1100)_2$ is

a) 1011 (b) 1001

c) 0111 (d) 1010

ircuit that changes a code into a set of signals alled

encoder (b) decoder

multiplexer (d) dataselector

ecimal counter has ———— states.

5 (b) 10

15 (d) 20

error in the D/A converter output may be due

Errors in the values of resistors used

Monotoncity

Small resolution

Its higher D/A speed

PART B — (5 × 5 = 25 marks)

swer ALL questions, choosing either (a) or (b).

h answer should not exceed 250 words.

Encode the decimal number to excess – 3 code.

(i) 46

(ii) 327.89

(iii) 20.305.

Or

3. The Boolean equation $\overline{\overline{A}+\overline{B}+\overline{C}}$ is equivalent to

(a) A B C (b) A + B + C

(c) $\overline{A}\cdot\overline{B}\cdot\overline{C}$ (d) $\overline{A+B+C}$

4. The most suitable gate for comparing two bits is

(a) AND (b) OR

(c) NAND (d) EX-NOR

5. The flip flop which produces unpredictable output for the inputs 1, 1 is

(a) R – S flipflop (b) J – K flipflop

(c) M – S flipflop (d) D flipflop

6. Circuit which consist of a quasistable state is called

(a) bistable circuit (b) monostable circuit

(c) tristable circuit (d) tristate circuit

7. Four adjacent '1"s in a Karnaugh map forms a

(a) Octet (b) Singlet

(c) Pair (d) Quad

(b) Determine the decimal numbers represented by the following binary numbers.

(i) 110101

(ii) 101101

(iii) 11111111

(iv) 00000000.

12. (a) Describe the positive logic and negative logic systems.

Or

(b) Explain EXOR gate with truth table.

13. (a) Explain the full subtractor with a circuit.

Or

(b) Discuss briefly 555 timer.

14. (a) Explain product of sum (POS) form of logical expression.

Or

(b) Discuss don't care condition.

15. (a) Define (i) shift register (ii) counter.

Or

(b) Define (i) resolution and (ii) linearity of D/A converter.

[P.T.O]

PART C — (5 × 8 = 40 marks)

Answer ALL questions, choosing either (a) or (b).

Each answer should not exceed 600 words.

16. (a) Perform the following subtraction using 2's complement method.

(i) 01000 – 01001

(ii) 01100 – 00011

(iii) 0011.1001 – 0001.1110.

Or

(b) Explain ASCII code.

17. (a) State and prove Demorgan's theorem.

Or

(b) Explain NOR as universal building block.

18. (a) Explain the operation of a JK flipflop.

Or

(b) Explain monostable multivibrator.

19. (a) Make a K-map for the function

$f = AB + A\overline{C} + C + AD + A\overline{B}C + ABC.$

Or

(b) Explain multiplexer with a diagram.

20. (a) Explain ring counter with a diagram.

Or

(b) Explain term :

(i) resolution

(ii) conversion time of A/D converter.

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